AMENDMENTS TO THE CLAIMS

The following Listing of Claims replaces all prior versions and listings in the Application.

Listing of Claims:

Claim 1 (Currently amended): A device ~~applied to~~ for applying a scaling factor ~~of~~ to a horizontal scan of a scanner [[,]] comprising ~~mainly~~:

a switching device having a first input terminal and a second input terminal, said switching device receiving at said first input terminal thereof an input ~~conducting wire situated at the foremost end of a scanner and used as an input end~~ ~~of~~ signal including a number of bits, said switching device having an output terminal producing thereat a signal selected from said input signal and a second signal responsive to a first clock cycle number;

an addition device ~~connected to said input~~ having a first input terminal and a second input terminal and operable to produce at an output terminal thereof a sum of a signal provided to said first input terminal and a signal provided to said second input terminal, said output terminal coupled to said second input terminal of said switching device and providing thereto said second signal ~~conducting wire~~;

a shifting device ~~with one end thereof connected to said input conducting wire~~ having an input terminal coupled to said output terminal of said switching

device and ~~the other end~~ having an output terminal coupled to said second input terminal of ~~thereof connected to~~ said addition device, said shifting device being operable to produce at said output terminal thereof said selected signal shifted a number of bits corresponding to a clock cycle number; and

an output terminal coupled to said output terminal of said shifting device and providing thereat ~~a shifter with one end thereof connected to said addition device and the other end thereof connected to~~ an output ~~conducting wire~~ signal upon a second clock cycle number.

Claim 2 (Original): The device as claimed in claim 1, wherein said shifting device is formed by winding conducting wires.

Claim 3 (Original): The device as claimed in claim 2, wherein said shifting device is a bus shifting circuit formed of logical gates.

Claims 4 - 6 (Canceled).

Claim 7 (Currently amended): A method ~~applied to~~ for applying a scaling factor ~~of~~ to a horizontal scan of a scanner [[,]] comprising ~~mainly~~ the steps of:

providing ~~transferring~~ an input signal including a sequence of pixel values, each of said pixel values being represented by a predetermined number of bits; ~~to~~

~~an addition device and a shifting device~~ [[,]]

right-shifting said input signal ~~n~~ *t* bits to produce a shifted signal ~~and then transferring to said addition device by said shifting device~~;

adding said input signal and said shifted signal to produce a summed signal ~~and an output signal of said shifting device by said addition device~~; and

changing the value of *t* prior to said summed signal right-shifting step;

right-shifting said summed signal a number of bits equal to the value of *t* to produce a t-shifted signal;

adding said summed signal to said t-shifted signal to produce a new summed signal;

repeating the method at said value of *t* changing step with said new summed signal as said summed signal until a predetermined number of cycles have been executed; and

right-shifting ~~an output signal of~~ said ~~addition~~ summed signal 2 bits to produce an output signal ~~and then outputting the result by said shifting device~~.

Claim 8 (Canceled).

Claim 9 (Currently amended): The method as claimed in claim 7 ~~8~~, wherein the ~~value of~~ method repeating step includes the step of setting said predetermined number of cycles to $(\log_2 n - 1)$, where n is at least 2^i more than the predetermined

number of bits ~~of~~ representing a pixel in said input signal, *i* being an integer.

Claims 10 - 11 (Canceled).

Claim 12 (Currently amended): A device applied to scaling factor of horizontal scan of a scanner, comprising mainly:

an input ~~conducting wire situated at the foremost end of a scanner and used as an~~ operable to receive an input ~~end of~~ signal;

at least an adder connected to said input ~~conducting wire~~;

at least a shifter with ~~one end~~ an input terminal thereof connected to said input ~~conducting wire~~ and ~~the other end~~ an output terminal thereof connected to an input of said adder; and

~~a~~ an end shifter with ~~one end~~ an input terminal thereof connected to said adder and ~~the other end~~ an output terminal thereof connected to an output operable to produce thereat an output signal ~~conducting wire~~.

Claim 13 (Original): The device as claimed in claim 12, wherein said shifter is formed by routing wires.

Claim 14 (Original): The device as claimed in claim 12, wherein said shifter is a bus shifting circuit formed of logical gates.

Claim 15 (Canceled).

Claim 16 (New): The device as claimed in claim 1, wherein said switching device is a multiplexer.

Claim 17 (New): The device as claimed in claim 1, wherein said first clock cycle number is one and said second clock cycle number is $(\log_2 n - 1)$, where n is at least 2^i more than said predetermined number of bits, and i is an integer.

Claim 18 (New): The method as claimed in claim 7, where said t incrementing step includes the step of changing t by a factor of 2.

Claim 19 (New): The device as claimed in claim 12, wherein said at least an adder includes a plurality of series-connected adders and said at least a shifter includes a plurality of shifters, each of said series-connected adders coupled at a first input thereof to an output of an adjacent one of said plurality of adders and coupled at a second input thereof to an output of a corresponding one of said plurality of shifters, said corresponding shifter being coupled at an input thereof to said output of said adjacent adder, said end shifter being coupled at an input thereof to an output of a last one of said plurality of adders.

Claim 20 (New): The device as claimed in claim 19, where said plurality of adders and said corresponding plurality of shifters are equal in number to at least $(\log_2 n - 1)$, where n is at least 2^i more than a predetermined number of bits of said input signal representing a pixel, i being an integer.